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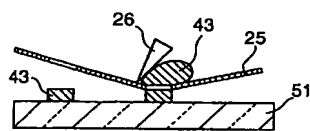
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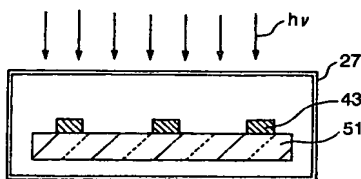
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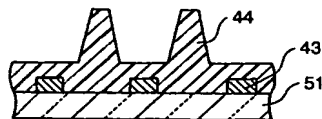
(54) Title: **MANUFACTURING PROCESS OF SUBSTRATE FOR IMAGE DISPLAY PANEL**



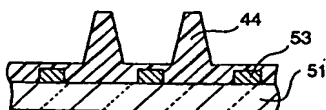
A



B



C



D

(57) Abstract: A manufacturing process of a substrate for an image display panel comprising a transparent substrate and protruding ribs and thin film electrodes each formed on the surface of the substrate in the predetermined pattern, in which the process comprises the steps of forming an electrode precursor layer by coating an electrode precursor on the surface of the substrate in the predetermined pattern, forming a rib layer in the predetermined pattern on the surface of the substrate on which the electrode precursor layer has been formed, and sintering the electrode precursor layer and the rib precursor layer simultaneously at the predetermined temperature.



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